Low Power Paradigm Featuring Dual Dynamic Node Pulsed Hybrid Flip-Flop With Dual Mode Logic and Clock Gating

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Abstract -- Today's technologies make possible powerful computing devices with multi-media capabilities. Consumer's attitudes are gearing towards better accessibility and mobility. In this paper, the objective is to develop a 4-b Johnson up-down counter that incorporates low power dual dynamic node pulsed hybrid flip-flop (DDFF), featuring dual mode logic (DML) and clock gating. The dual dynamic node hybrid flip-flop eliminates the large capacitance present at the pre-charge node of other designs by following a split dynamic node structure to separately drive the output pull-up and pull-down transistors. The dual mode logic allows a fly change between two operational modes at the gate level: static mode and dynamic mode. The power consumption is controlled further by clock gating. The analysis approach reveals the sources of performance and power consumption bottlenecks in different design styles. The performance improvements indicate that the proposed designs are well suited for modern high-performance designs where power dissipation and delay are of major concern. The simulation results are compared using T-Spice.

Index Terms— Low power, DDFF, high speed, DML, clock gating

1 INTRODUCTION

The building of Low Power VLSI systems has been emerged as they are very high in demand because of the rapid growth in technologies. Power consumption plays an important role in any integrated circuit and is listed as one of the top three challenges in International technology roadmap for semiconductors. In any integrated circuit, flip-flop consumes large amount of power as they make maximum number of internal transitions.

PowerPC 603 is one of the most efficient classic static structures. The large D-Q delay and CLK node capacitances make the design inferior in performance. SDFF is the fastest classic hybrid structure, but is not efficient as far as power consumption is concerned because of the large CLK load as well as the large pre-charge capacitance. The Hybrid Latch Flip-Flop (HLFF) is not the fastest but has a lower power consumption compared to the SDFF. The conditional data mapping flip-flop (CDMFF) is one of the most efficient among them but the additional transistors added for the conditional circuitry make the flip-flop bulky and cause an increase in power dissipation. A cross charge control flip flop (XCFF) has considerable advantages over SDFF and HLFF in both power and speed but it is not very efficient due to the susceptibility to charge sharing at the internal dynamic nodes.

The Dual Dynamic node hybrid Flip-Flop (DDFF) eliminates the drawbacks of other designs and presents an area, power, and speed efficient method to incorporate complex logic functions into the flip-flop. The existing design of counter includes static 2-input multiplexer where power consumption is of major concern. In order to magnify the performance improvement, we propose a 4-b Johnson up/down counter with dual mode logic and clock gating. The normal multiplexer has been replaced by DML multiplexer where the counter could be operated both in static mode as well as dynamic mode.

The rest of this paper is divided as follows. Section II discusses the disadvantages of existing flip-flop structures and challenges in achieving high performance. In section III, the proposed 4-b Johnson up/down counter incorporating DML logic and its operation are provided. Section IV describes the proposed 4-b Johnson up/down counter with clock gating. Section V includes the performance analysis and simulation result comparisons. In section VI, we conclude with the improvements of the proposed designs over the existing modern high performance designs.

2 ANALYSIS OF FLIP-FLOP STRUCTRES

The field of complementary metal–oxide semi-conductor (CMOS) integrated circuits has reached a level of maturity where it is now a mainstream technology for higher integration density, lower power consumption, and high-speed capability. Latches and flip-flops are the basic elements for storing information. The flip-flops and latches could be grouped under the static and dynamic design styles. The former type of designs dissipates lower power and the latter type includes the modern high performance flip-flops.

PowerPC 603 is one of the most efficient classic static structures. It has the advantages of having a low power keeper structure and a low latency direct path. The large data and CLK node capacitances make the design inferior in performance as shown in fig. 1.

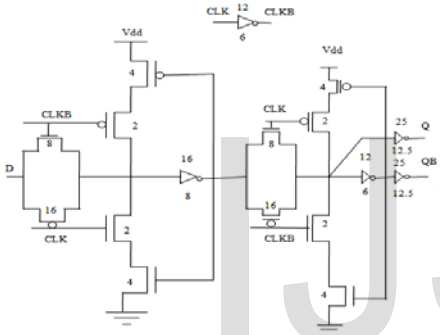

Figure 1: Power PC 603 flip-flop

The Semi-dynamic flip-flop **(**SDFF) is the fastest classic hybrid structure, but is not efficient as far as power consumption is concerned because of the large CLK load as well as the large pre-charge capacitance as shown in fig. 2.

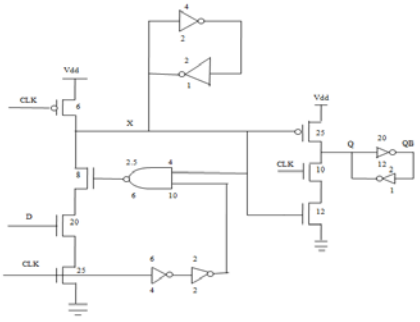

Figure 2: Semi-dynamic flip-flop

The significant advantage over HLFF is that there is very little performance penalty for embedded logic functions. The disadvantages are bigger clock load and larger effective pre-charge capacitance, which results in increased power consumption for data patterns with more "ones."

Hybrid Latch Flip-Flop is one of today's high-performance flip-flops. HLFF is not the fastest but has a lower power consumption compared to the SDFF. The longer stack of nMOS transistors at the output node makes it slower than SDFF and causes large hold-time requirement as shown in fig. 3.

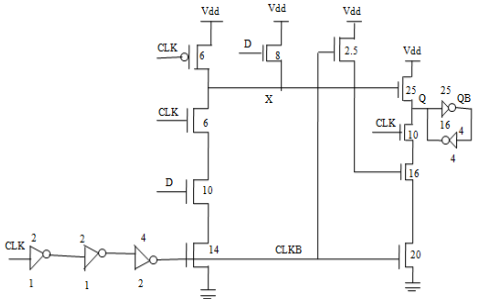

Figure 3: Hybrid latch flip-flop

This large positive hold- time requirement makes the integration of HLFF to complex circuits a difficult process. Also it is inefficient in embedding logic.

The conditional data mapping flip-flop (CDMFF) is one of the most efficient among other flip-flops. It uses an output feedback structure to conditionally feed the data to the flip-flop as shown in fig. 4. This reduces overall power dissipation by eliminating unwanted transitions when a redundant event is predicted.

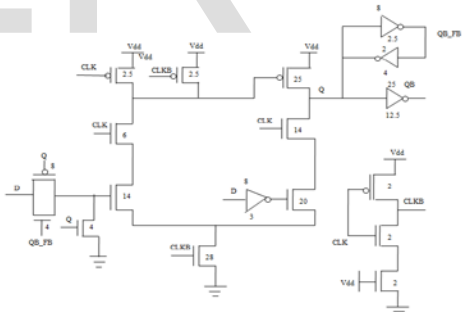

Figure 4: Conditional data mapping flip-flop

The additional transistors added for the conditional circuitry make the flip-flop bulky and cause an increase in power dissipation at higher data activities.

The cross charge control flip-flop (XCFF) is a low power and high-speed flip-flop. It has two dynamic nodes driving output transistors separately as shown in fig. 5. The power-delay product of the XCFF is smaller than that of CMOS flip-flop and the semi-dynamic flip-flop (SDFF).

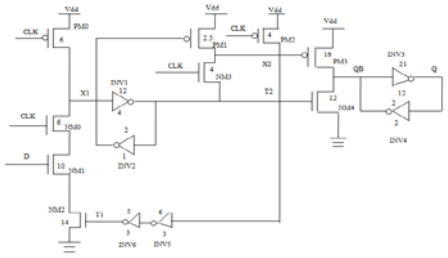

Figure 5: Cross charge control flip-flop

This effect of charge sharing becomes uncontrollably large when complex functions are embedded into the design.

The Dual Dynamic node pulsed hybrid Flip-Flop (DDFF) is used to decrease circuit complexity, increasing operating speed and lower power dissipation. The glitch problems resulting from charge sharing could be reduced. An unconditional shutoff mechanism in DDFF overcomes the drawback of XCFF as shown in fig. 6.

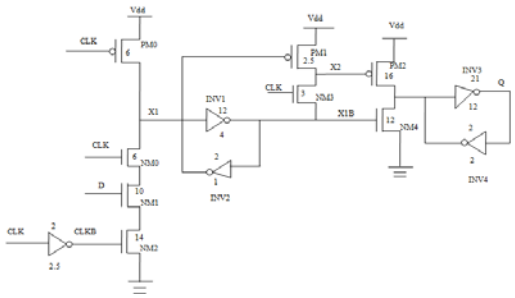

Figure 6: Dual dynamic node hybrid flip-flop

The 4-b Johnson up/down counter is designed with a set of 2-input multiplexers and flip-flops (DDFF) as shown in fig. 7.

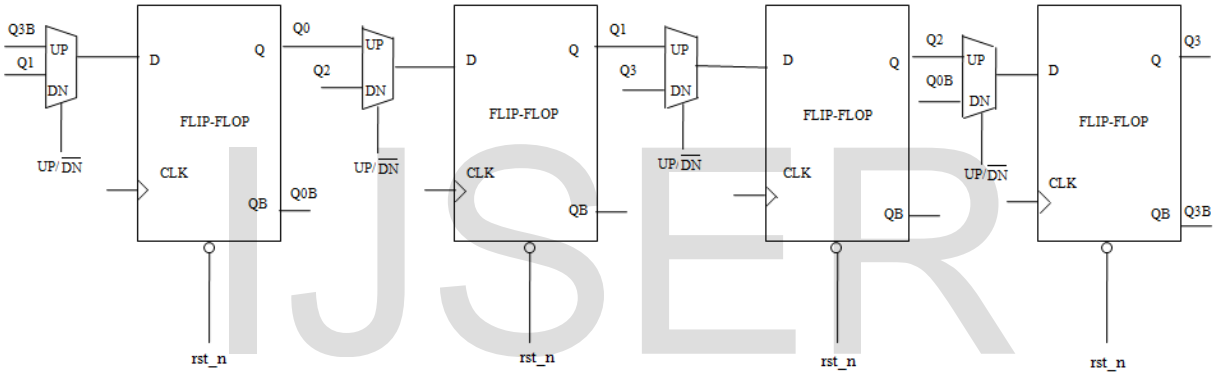

Figure 7: Schematic of 4-b Johnson up-down counter

When the Johnson counter is first initialized, the only asserted piece of wire is the one connecting the complemented output of the last flip-flop to the input of the first flip-flop in the counter. Then as the clock cycles, the signal originating from the first flip-flop propagates though all the flip-flops until it reaches the output node.

3 PROPOSED 4-B JOHNSON UP-DOWN COUNTER WITH DML

The dual mode logic (DML) enables a very high level of energy-delay optimization flexibility at the gate level. In this paper, this flexibility is utilized to improve energy efficiency and performance of circuits. It can be switched between static and dynamic modes of operation according to system requirements and thus support applications in which a flexible workload is required as shown in fig. 8. In the static mode, DML gates consume very low energy with some performance degradation, as compared to standard CMOS gates. Alternatively, dynamic DML gates operation obtains very high performance at the expense of increased energy dissipation.

The basic concept behind the DML is to combine the traditional CMOS logic (or any other static logic) with a dynamic logic. Energy efficiency is achieved in the static DML mode at the expense of slower operation (Low Energy and Low Performance). However, the dynamic mode is characterized by high performance with increased energy consumption (High Energy and High Performance).

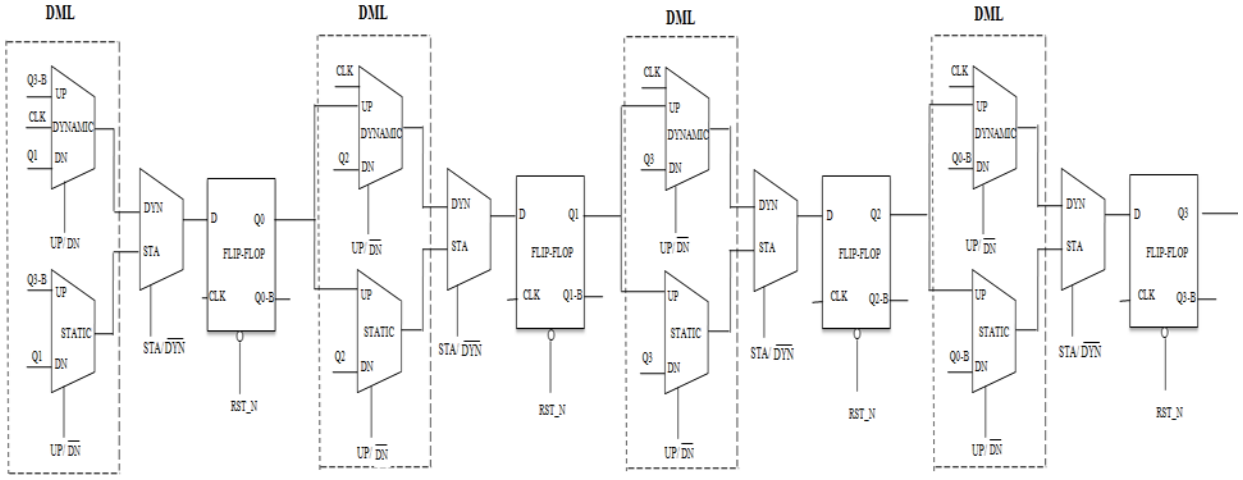

Figure 8: 4-b Johnson up/down counter with Dual Mode Logic

The 4-b Johnson up/down counter comprises of four dual dynamic node pulsed hybrid flip-flops (DDFF) and DML multiplexers. The DDFF serves to be highly energy efficient with reduced delay. Initially all the flip-flops are in a reset condition. During up count, Q3-B is high ('1') on both the static and dynamic multiplexers of DML. Depending on the mode of operation been selected through the selection lines (STA/DYN), inputs are given to the D-FF. Q0 is high ('1') and passes onto the next DML part of the counter. Similarly the process continues depending on the counter operation (up/down).

4 PROPOSED 4-B JOHNSON UP/DOWN COUNTER WITH CLOCK GATING

The power dissipation is reduced by deactivating the clock signal when there are no data transitions.

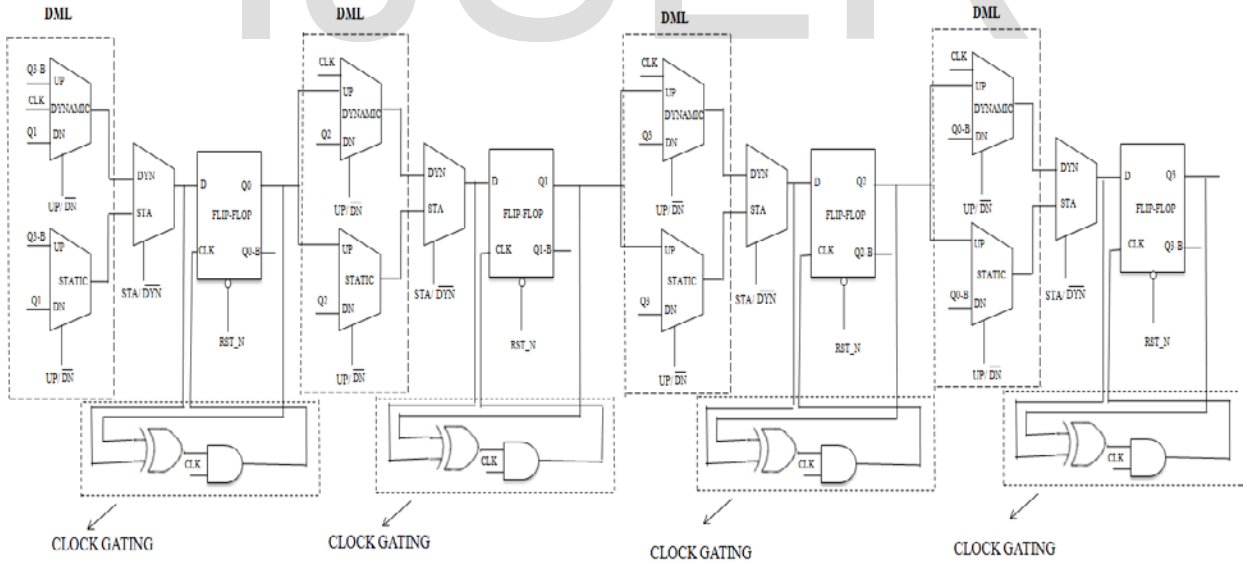

Figure 9: 4-b Johnson up/down counter with clock gating

In many applications, the power consumption of the IC clock system is one of the main sources of chip power dissipation. This is due to the high switching activity and the heavy capacitive loading of the clock network. Consequently, many techniques have been recently proposed to reduce clock system power dissipation.

In this paper, the power consumption is reduced due to the clock signal being deactivated (clock gating) when there are no transitions on the D input. The

comparison between D and Q is performed by an XOR gate, while the gating logic circuit compromises a simple AND gate as shown in fig. 9. The operation of the circuit is as follows. When D is different from Q, the gating logic enables the clock signal so that the flip-flop can correctly switch. And if D is equal to Q, the gating logic inhibits the propagation of switching activity. In this way the power consumption is reduced.

The analysis of the work is carried out using T-Spice. Power consumption and the speed performances are discussed for HLFF, CDMFF, XCFF, PowerPC 603, SDFF and DDFF. The data driving power, clock driving power, latching power and D-Q delay are the major parameters considered as shown in Table 1. The comparison results show that DDFF serves to be an efficient flip-flop and it is well suited for modern high performance systems.

5 PERFORMANCE ANALYSIS AND SIMULATION RESULTS

Table 1: Performance Analysis of Various Flip-Flop Structures

Flip-flop	Number of transistors	Data driving power(μW)	Clock driving power(μW)	Latching power (μW)	Total power (μW)	Minimum D-Q delay (ps)
SDFF	23	10.4376	27.8928	100.7269	139.0573	32689
HLFF	20	3.72038	2.57981	20.69455	26.99474	12228
PowerPC 603	22	34.11666	19.7447	18.02251	71.8838	30050
CDMFF	22	13.3110	6.44311	23.41135	43.16546	45500
XCFF	21	1.48397	7.21041	20.12574	28.82012	19820
DDFF	18	1.01776	5.43912	16.74268	23.19956	11740
DDFF-ELM	22	0.16070	6.15563	20.00010	26.31633	10050

Table 2: Performance of 4-B Johnson Up/Down Counter

Flip-flop	SDFF	HLFF	PowerPC 603	CDMFF	XCFF	DDFF
Power(μW)	484.475	352.76	379.623	298.321	267.562	155.811

The performance of 4-b Johnson up/down counter was analyzed by incorporating various design styles of flip-flops as shown in Table 2. The analysis reveals that the Dual Dynamic node pulsed hybrid Flip-Flop (DDFF) serves to be an efficient flip-flop structure by means of low power and high speed. The simulation of 4-b Johnson up-down counter is been carried out using S-Edit of T-Spice. The output waveforms generated were shown in fig. 10. (a,b,c,d).

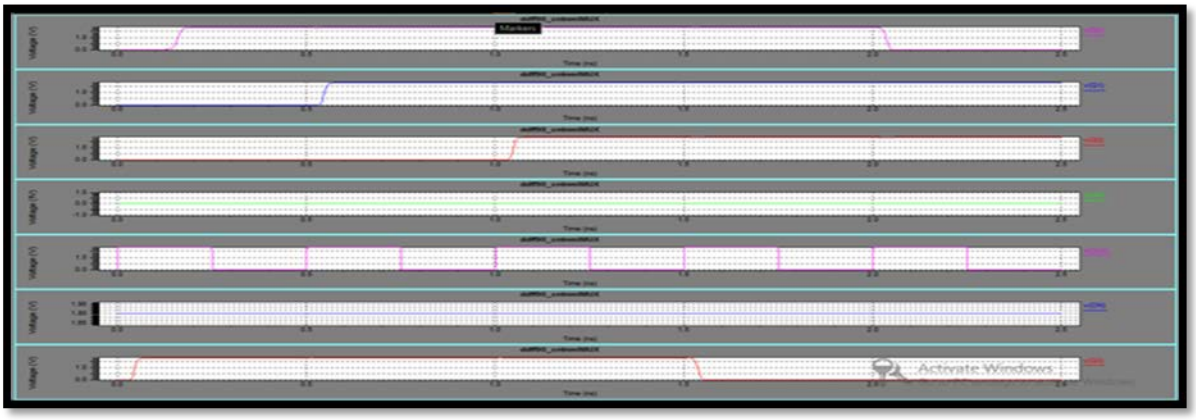

Figure 10(a): Simulation of 4-b Johnson up/down counter with normal multiplexer

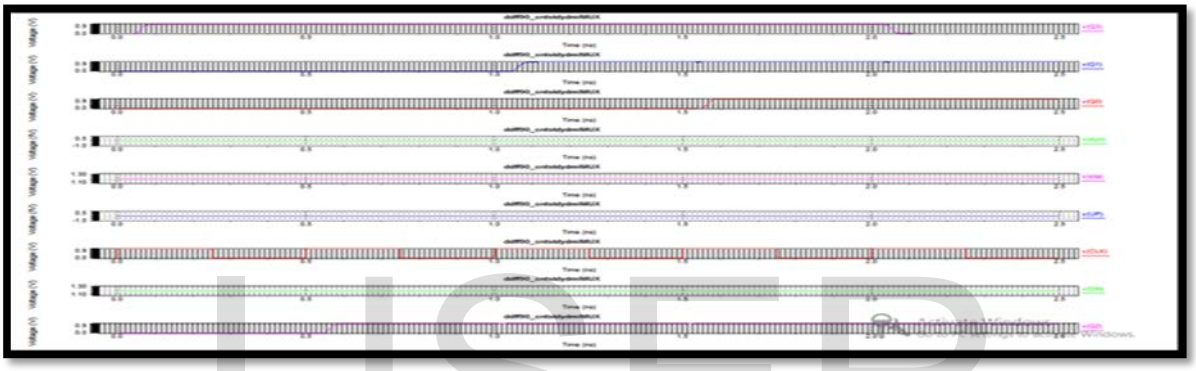

Figure 10(b): Simulation of 4-b Johnson up/down counter with DML (static) multiplexer

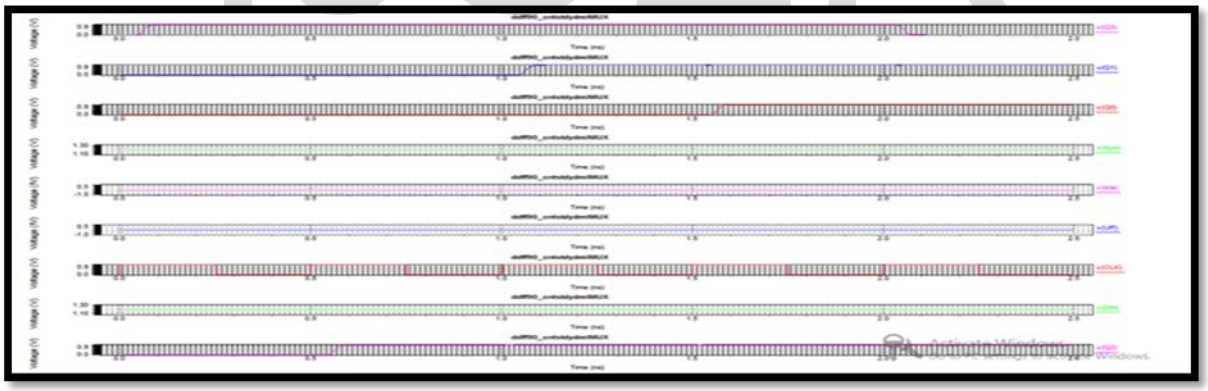

Figure 10(c): Simulation of 4-b Johnson up/down counter with DML (dynamic) multiplexer

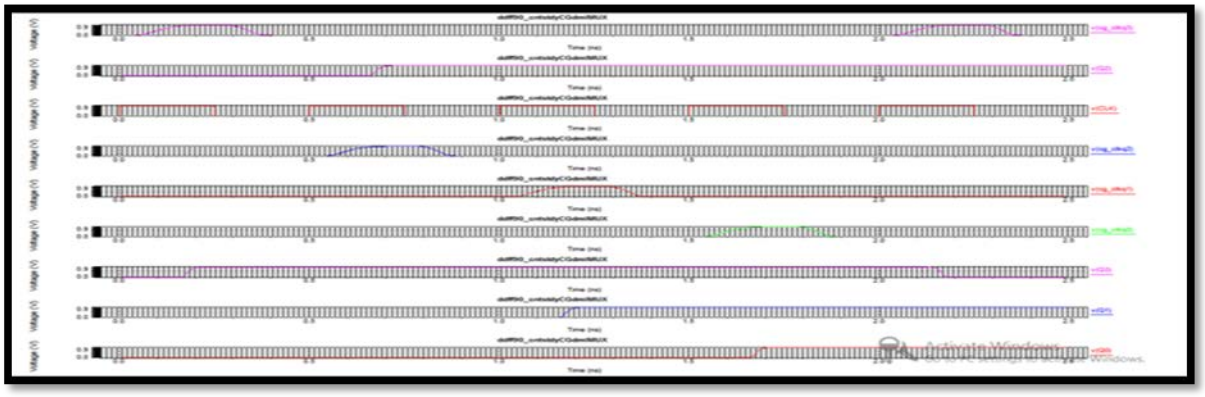

Figure 10(d): Simulation of 4-b Johnson up/down counter (DML) and clock gating

The clock gating controls overall power dissipation of the circuit. The clock signal stays high ('1') only during data transition in each flip-flop of the counter. Until any of the transition occurs, clock pulse will be maintained low ('0').The counter with normal multiplexer consumes more power when compared to DML multiplexer. The speed of the counter is also been degraded. While operating the counter in DML (static) mode, it serves to be energy efficient whereas in DML (dynamic) mode, it serves to perform with high speed as shown in Table 3.

The power consumption of 4-b Johnson up/down counter with clock gating /without clock gating are shown in Table 4. Further power dissipation of counter incorporating DML has been reduced through clock gating.

Table 3: Performance Analysis of 4-B Johnson Up-Down Counter with DML

COUNTER	NORMAL MUX	DML MUX (STATIC)	DML MUX (DYNAMIC)
POWER (µW)	1022	664	670
DELAY (ps)	507	490	486

Table 4: Power Consumption of 4-B Johnson Up-Down Counter with Clock Gating

DML	POWER WITHOUT CG (µW)	POWER WITH CG (µW)
STATIC MODE	664	647
DYNAMIC MODE	670	653

6 CONCLUSION

Thereby, various flip-flop structures were analyzed. Each design tends to be the superior one to the other due to certain advantages. The power dissipation and speed performances of the flip-flop structures are considered. The DDFF eliminates the redundant power dissipation present in XCFF. The simulation result shows an improvement in power and delay parameters. The efficiency of the flip-flop was highlighted using a 4-b Johnson up-down counter, respectively. Further flexibility were attained to improve energy efficiency and performance by incorporating a DML (Dual Mode Logic) and clock gating in it. It will also encourage further research on dual-edge triggered circuits and topologies.

REFERENCES

[1] Kalarikkal Absel, Lijo Manuel and R. K. Kavitha, 2013, 'Low Power Dual Dynamic Node Pulsed Hybrid Flip-Flop Featuring Efficient Embedded Logic', VLSI Systems, IEEE Transactions (Volume:21 Issue: 9)

[2] Ahmed Sayed and Hussain Al-Asaad , 2011, 'Low Power Flip-Flops: Survey, Comparative Evaluation and a New Design' , IACSIT International Journal of Engineering and Technology, Vol.3, No.3.

[3] Ismail.S.M and Islam.F.T., 2012, 'Low power design of Johnson Counter using clock gating' International Conference on Computer and Information Technology (ICCIT), pp 510-517

[4] Itamer Levi and Alexander Fish, 2013, 'Dual Mode Logic Design for energy efficiency and high performance', IEEE Access.

[5] Albert Ma and Krste Asanovi´c 'A Double Pulsed Set-Conditional Reset Flip-Flop' MIT Laboratory for Computer Science.

[6] Jae-Il Kim and Bai-Sun Kong, 2003, 'Dual Edge- Triggered NAND-Keeper Flip-Flop for High Performance VLSI' Journal of semiconductor technology and science, Vol 2.

[7] Klass.F ,1998 , 'Semi-dynamic and dynamic flip-flops with embedded logic' VLSI Circuits, Digest of Technical Papers, pp 108-109.

[8] Peiyi Zhao, Tarek K. Darwish and Magdy A. Bayoumi, 2004 , 'High Performance and Low Power Conditional Discharge Flip-Flop' IEEE transactions on Very Large Scale Integration (VLSI) systems, Vol. 12, no. 5.

[9] Venkadeshkumar.G and Pandiaraj.K , 2012, 'Design of Low Power Flip-Flop to Reduce Area and Delay Using Conditional Pulse Enhancement Method International Journal of Computer Applications on Electronics, Communication and Information Systems.

[10] Yuan.J and Svensson.C, 2002, 'New single-clock CMOS Latches and flip-flops with improved speed and power savings',Solid-State Circuits,(vol:32,Iss:1) pp-62-69.